(12) UK Patent Application (19) GB (11) 2 392 552 (13) A

(43) Date of A Publication 03.03.2004

(21) Application No: 0219887.7

(22) Date of Filing: 27.08.2002

(51) INT CL[7]:
H01L 23/367 , G02B 6/12

(52) UK CL (Edition W):
H1K KPDX K1EA K1EA1 K1EB K1ED K4C1T K5A4

(56) Documents Cited:
EP 0413182 A2 US 20020071188 A1

(58) Field of Search:
UK CL (Edition V) H1K
INT CL[7] G02B, H01L, H01S
Other: Online: EPODOC, JAPIO, INSPEC,WPI

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(54) Abstract Title: **Thermal isolation of optical chips**

(57) An optical chip unit (15) comprises an optical chip (31) having a lower side (30), and a carrier (27). The carrier has cut-out portions for thermal isolation of the optical chip. The optical chip may be an optical demultiplexer, for example an arrayed waveguide grating, and the optical circuit element may be a light source, an optical attenuator or an optical amplifier.

FIG. 4A

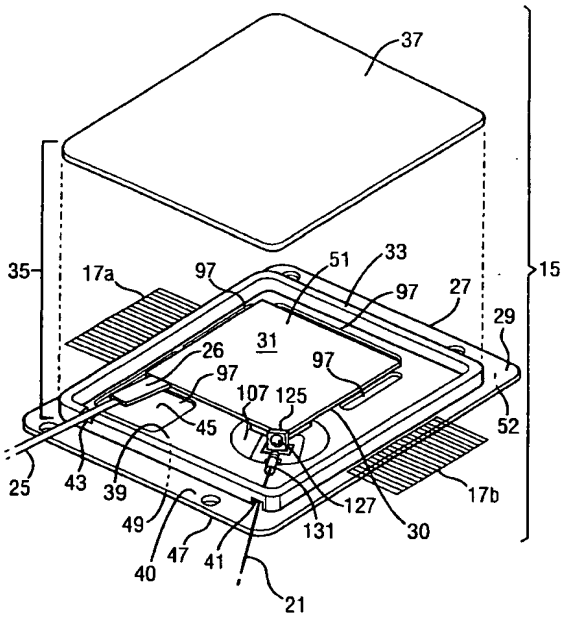

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FIG. 1

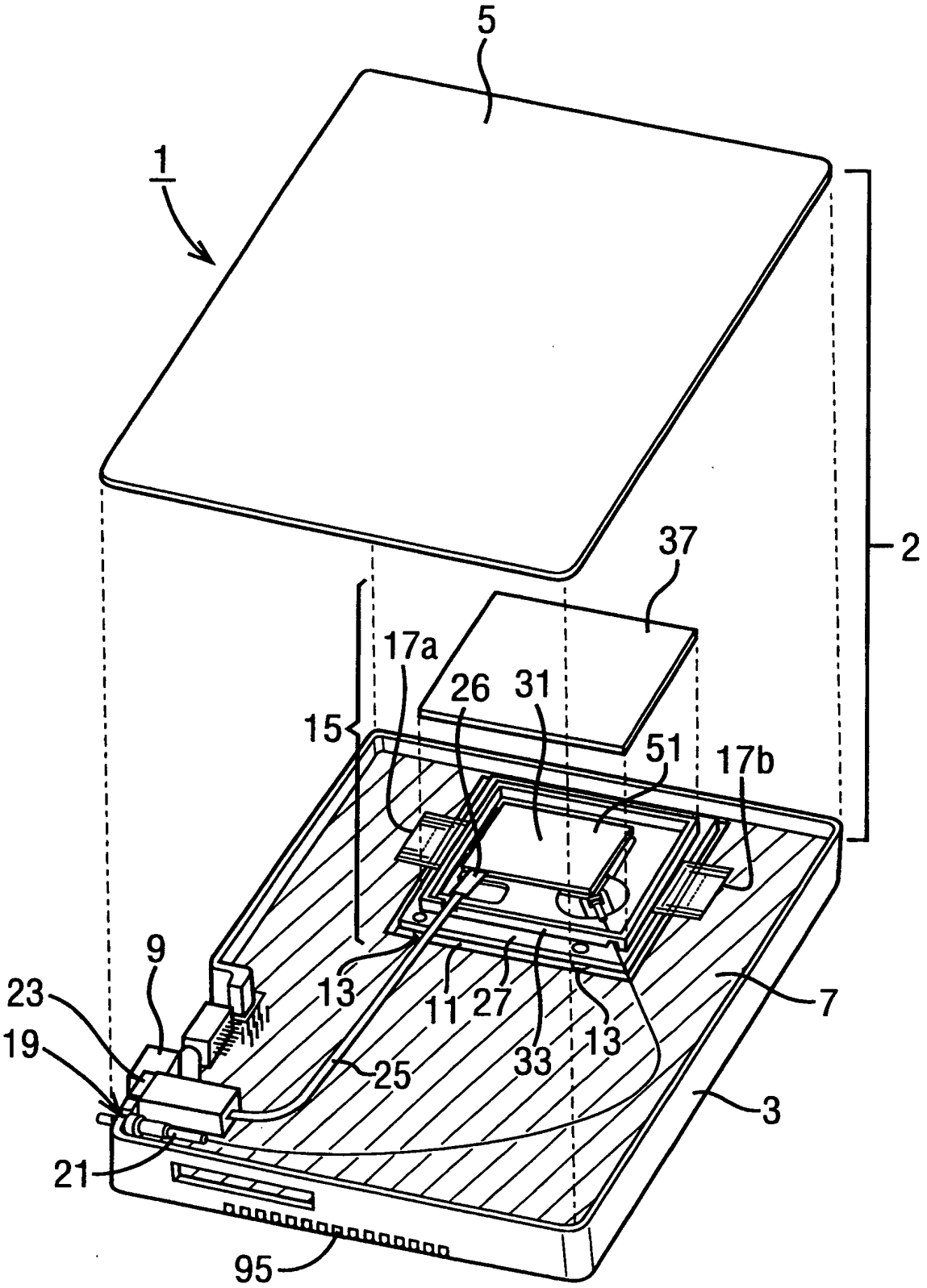

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FIG. 2

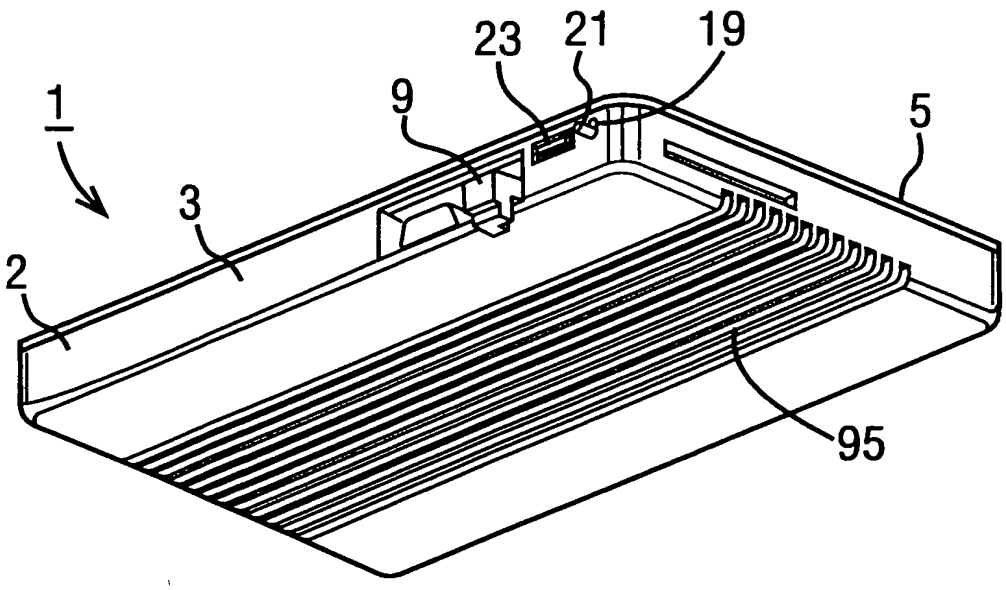

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FIG. 3

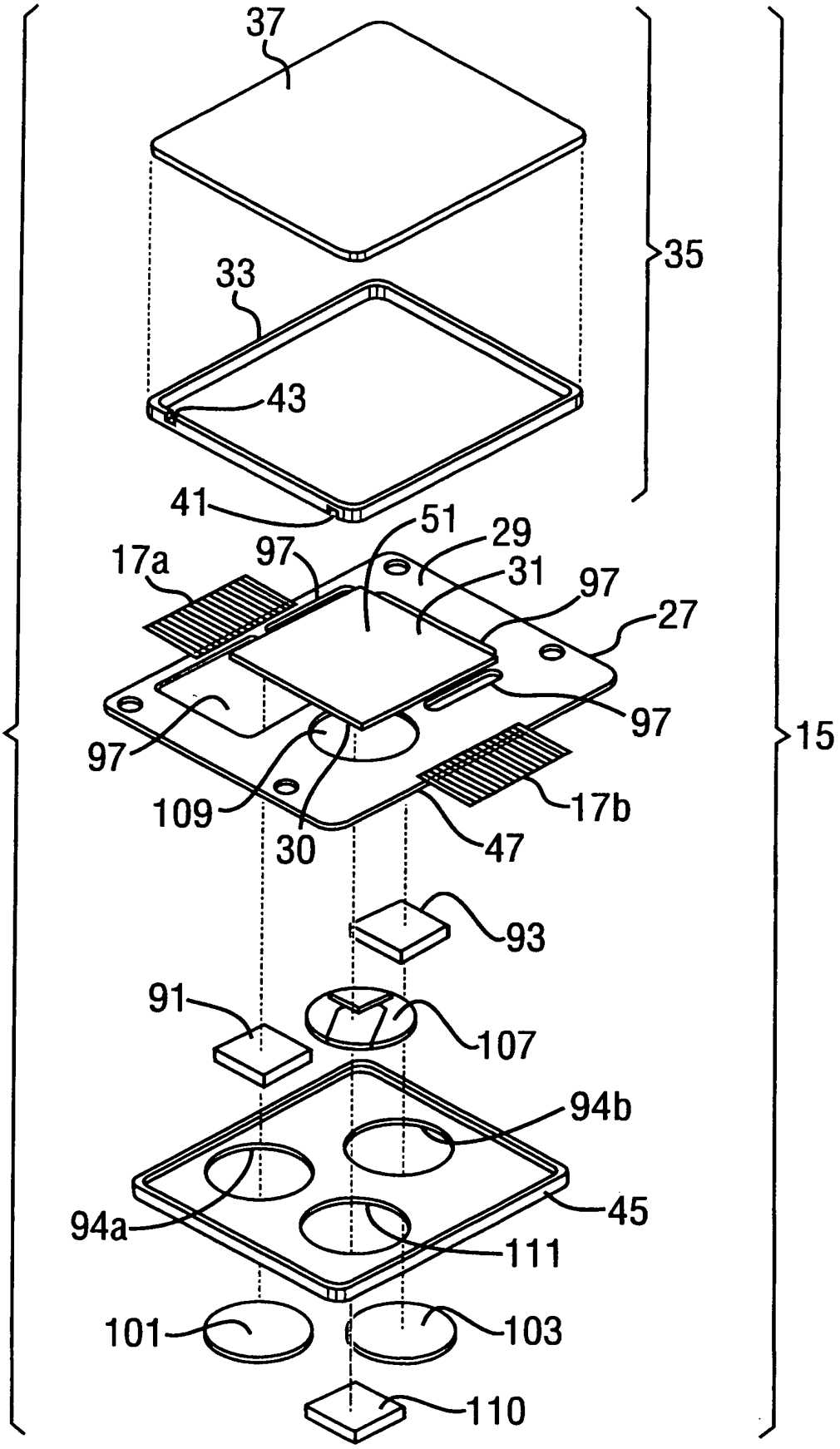

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FIG. 4A

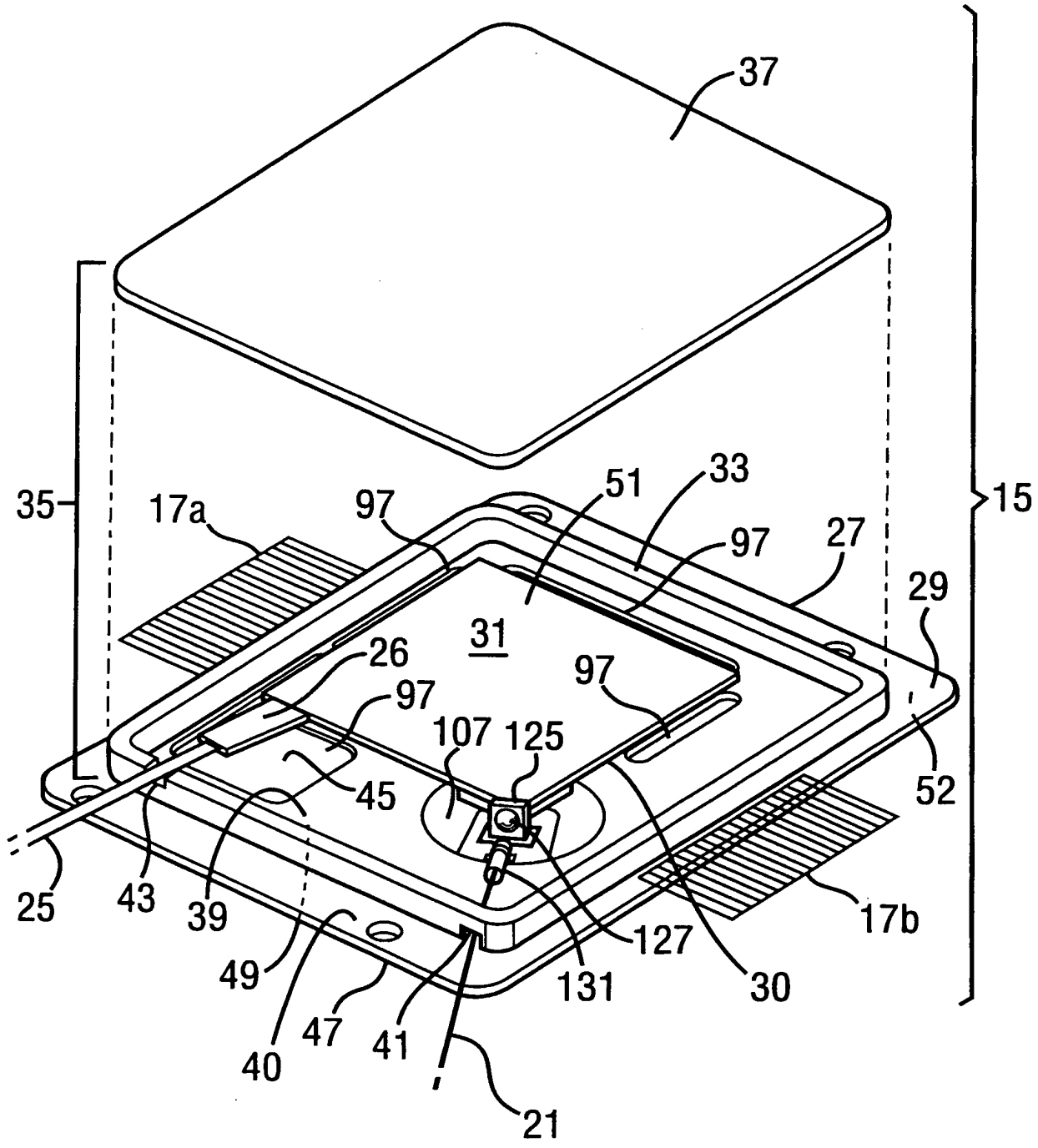

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FIG. 4B

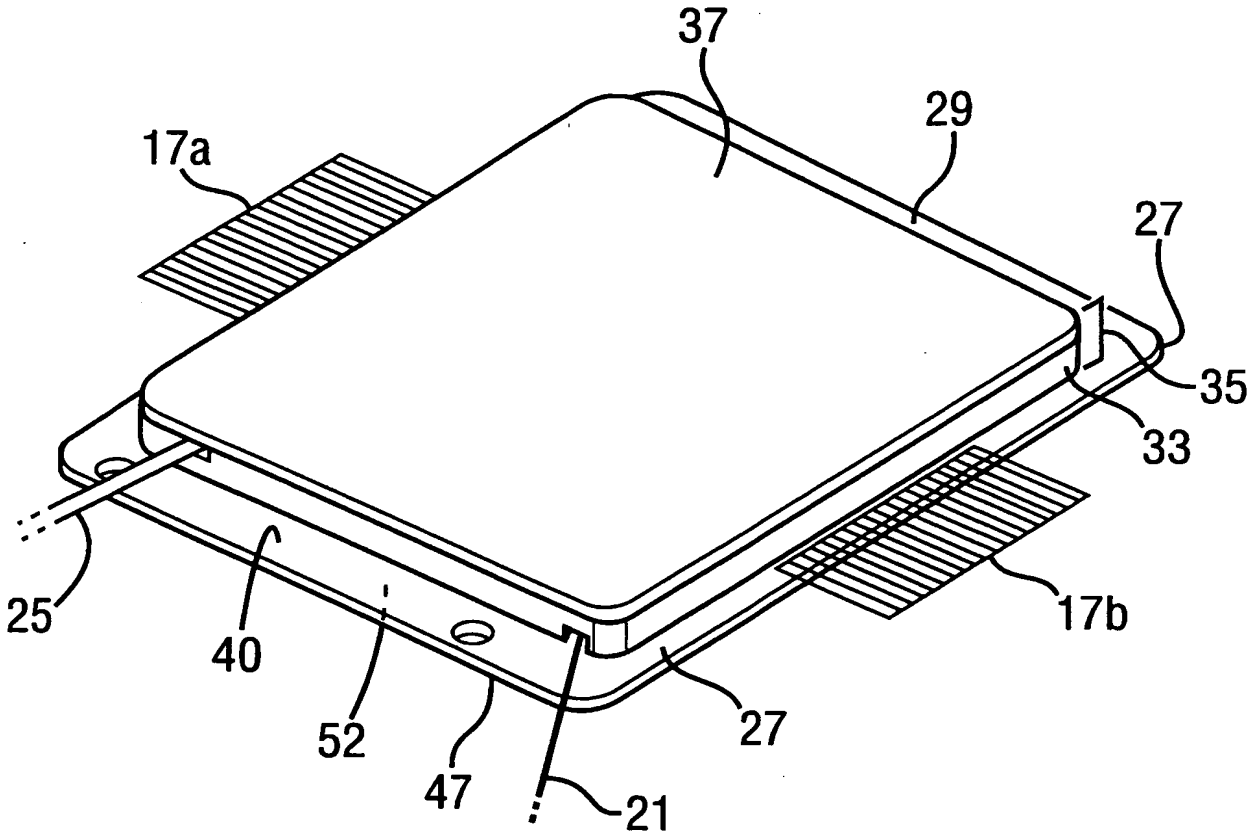

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FIG. 5

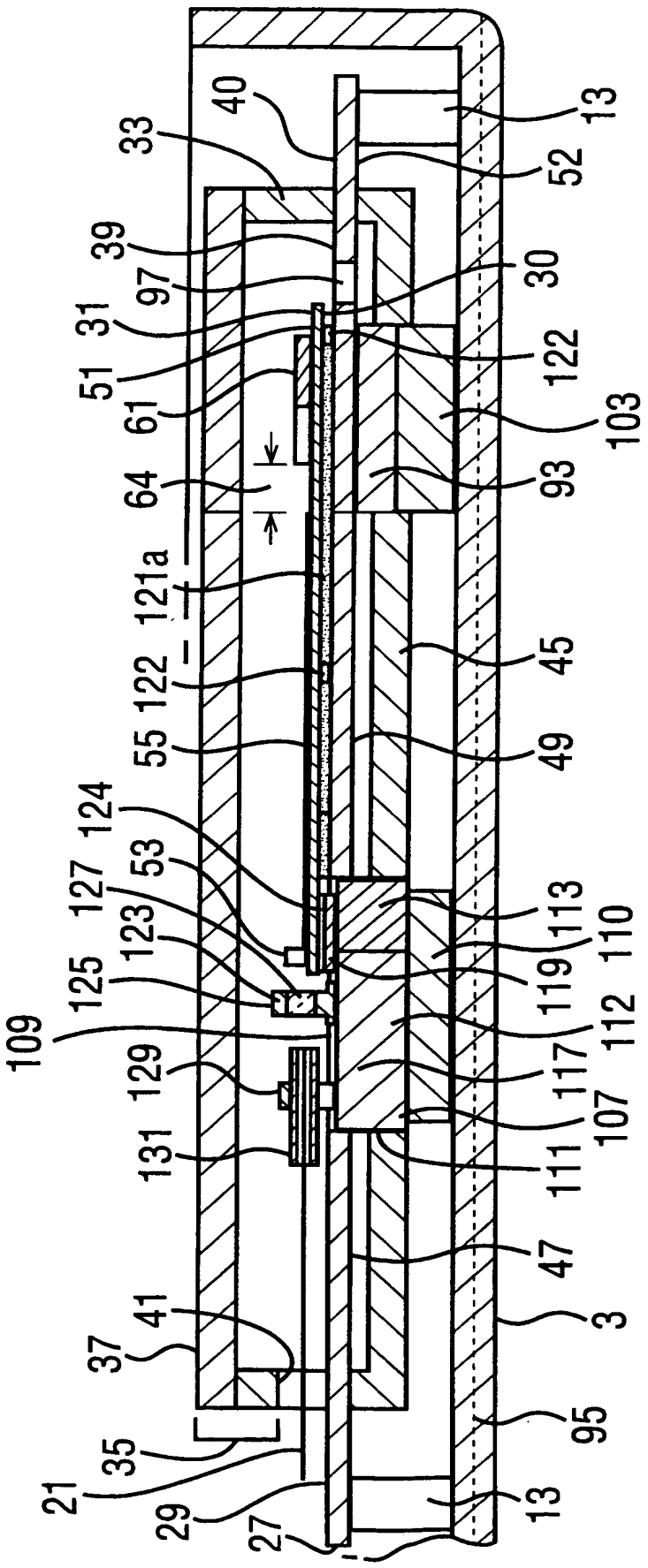

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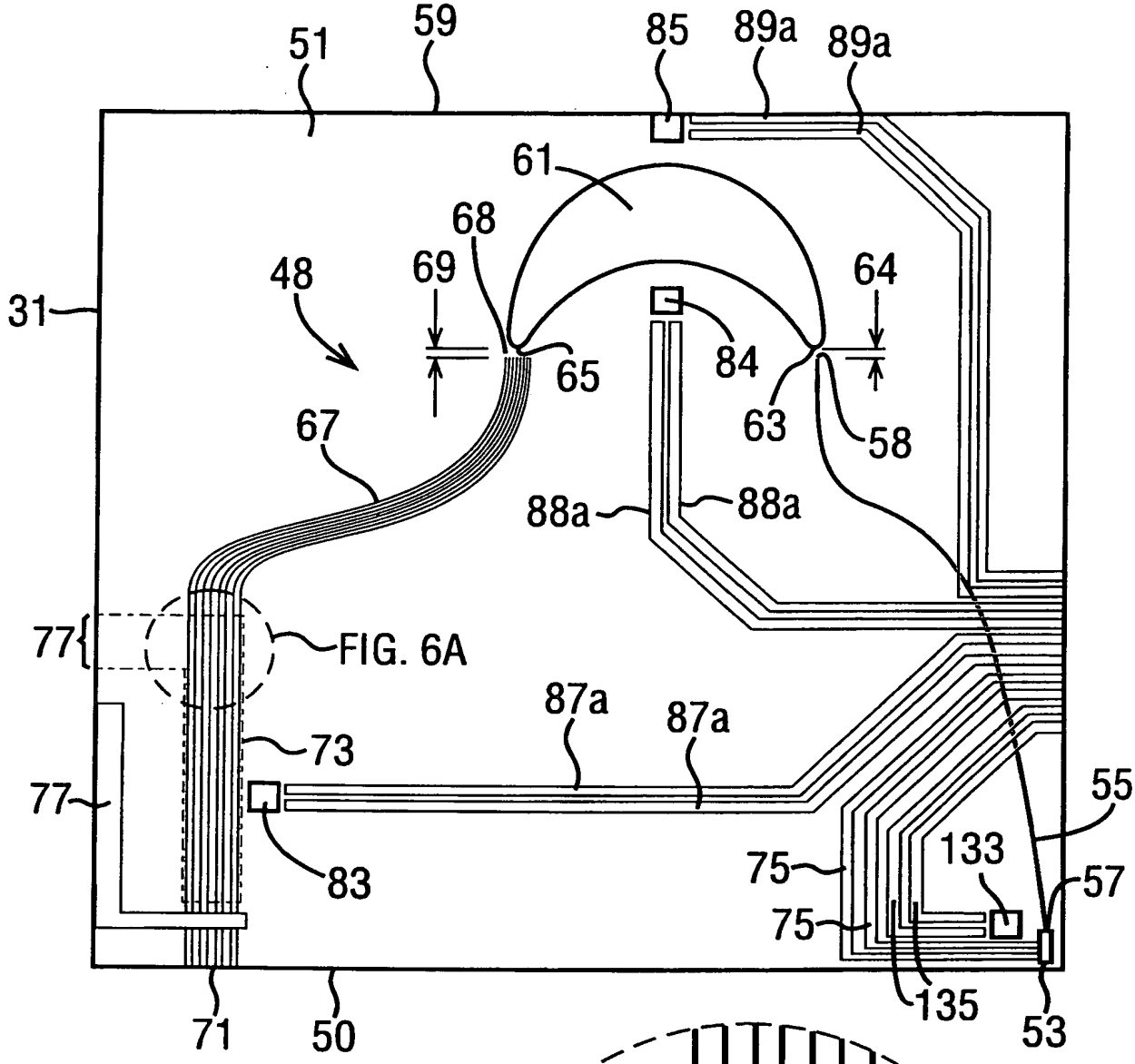
FIG. 6



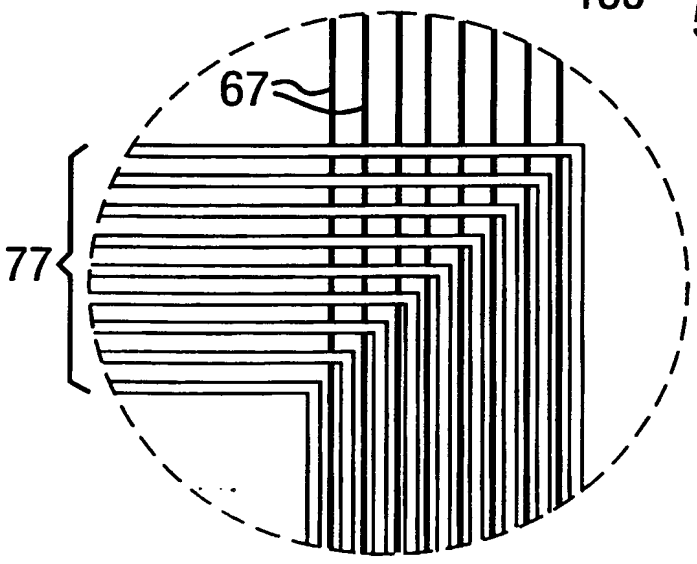


FIG. 6A

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FIG. 7

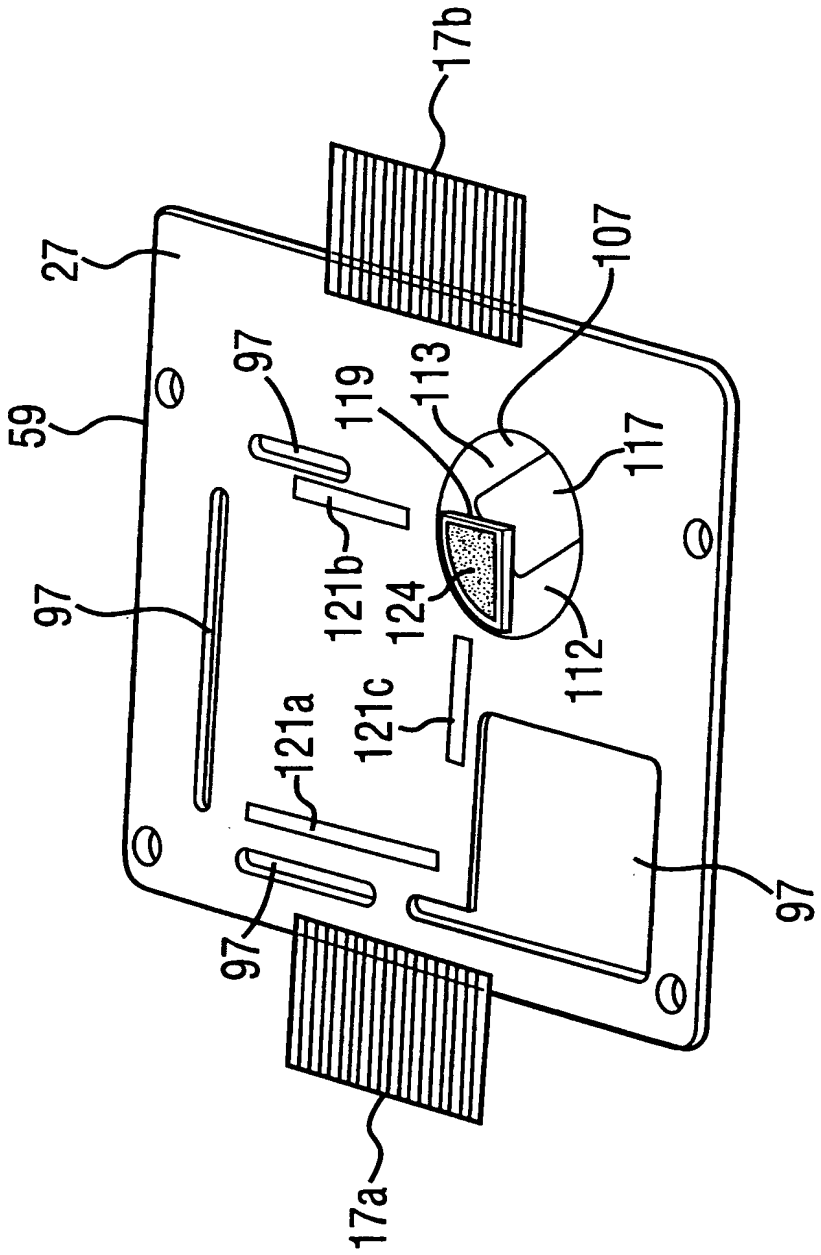

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FIG. 8

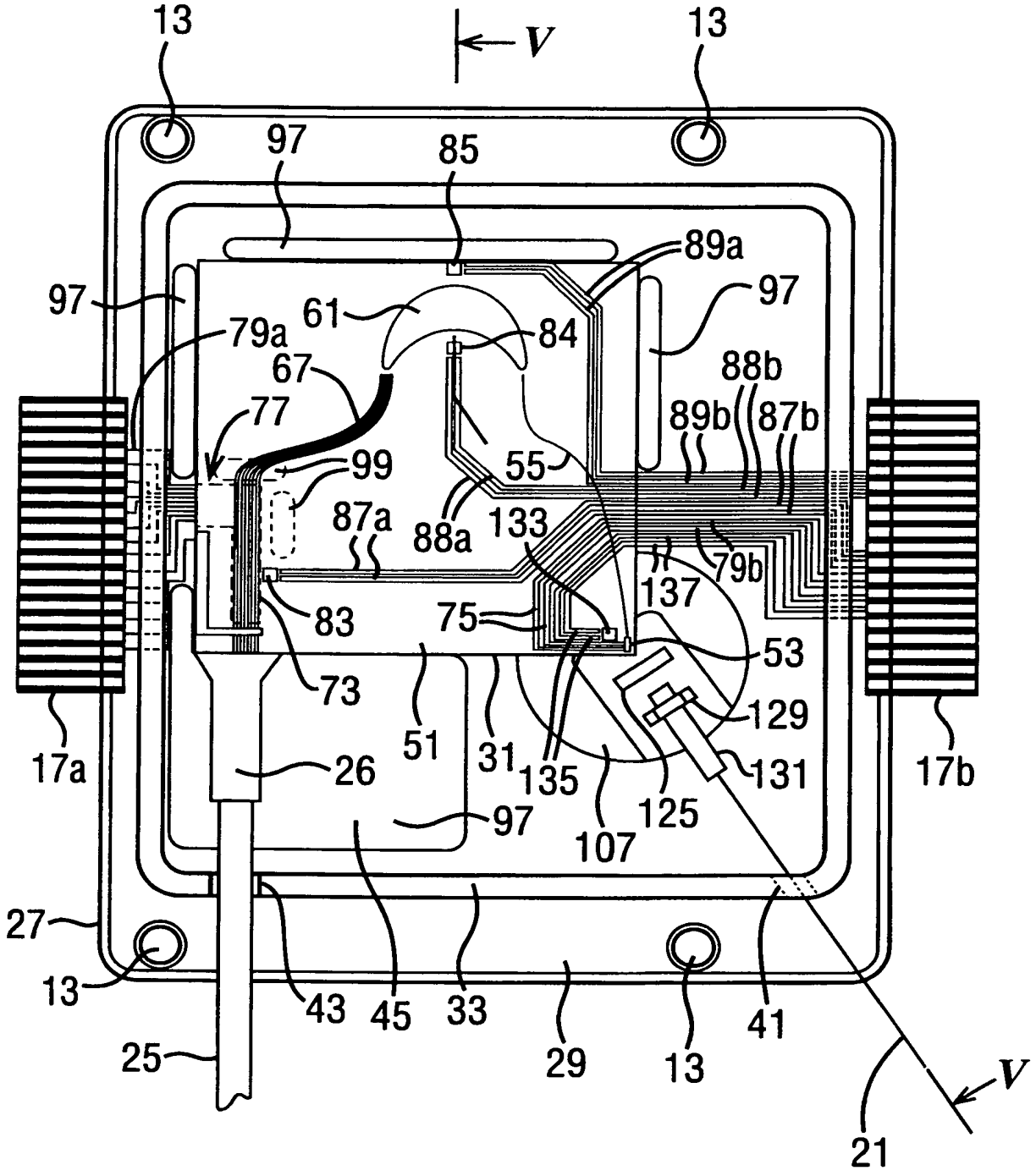

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FIG. 9A

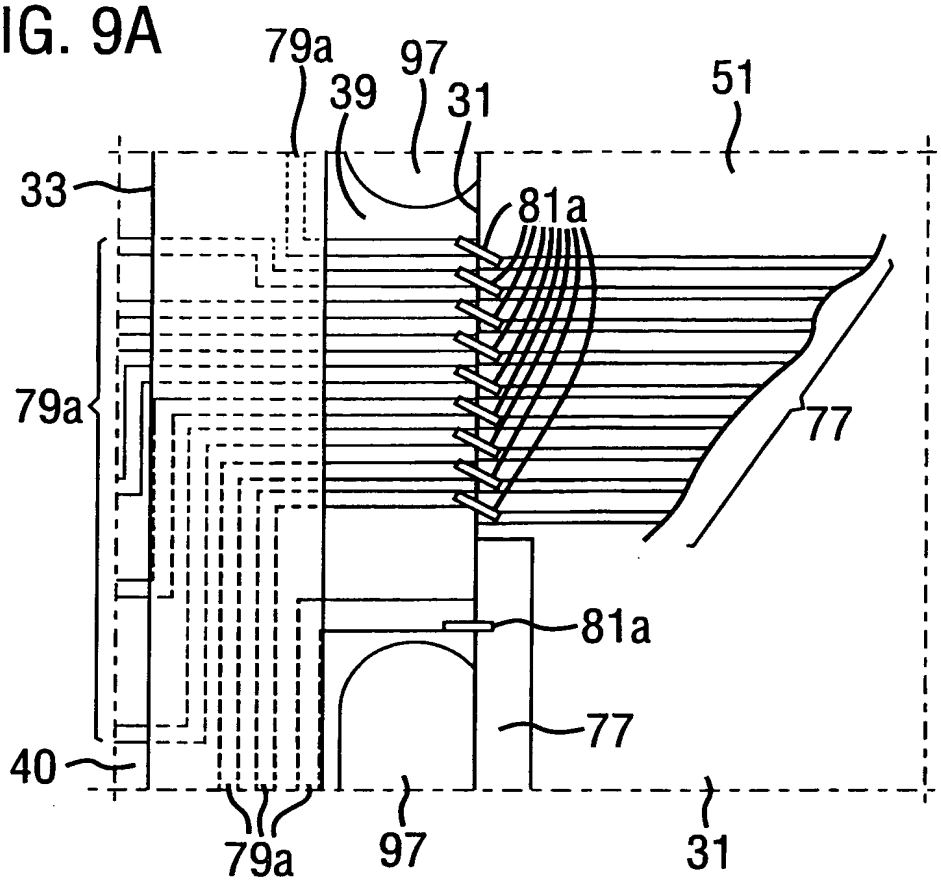

FIG. 9B

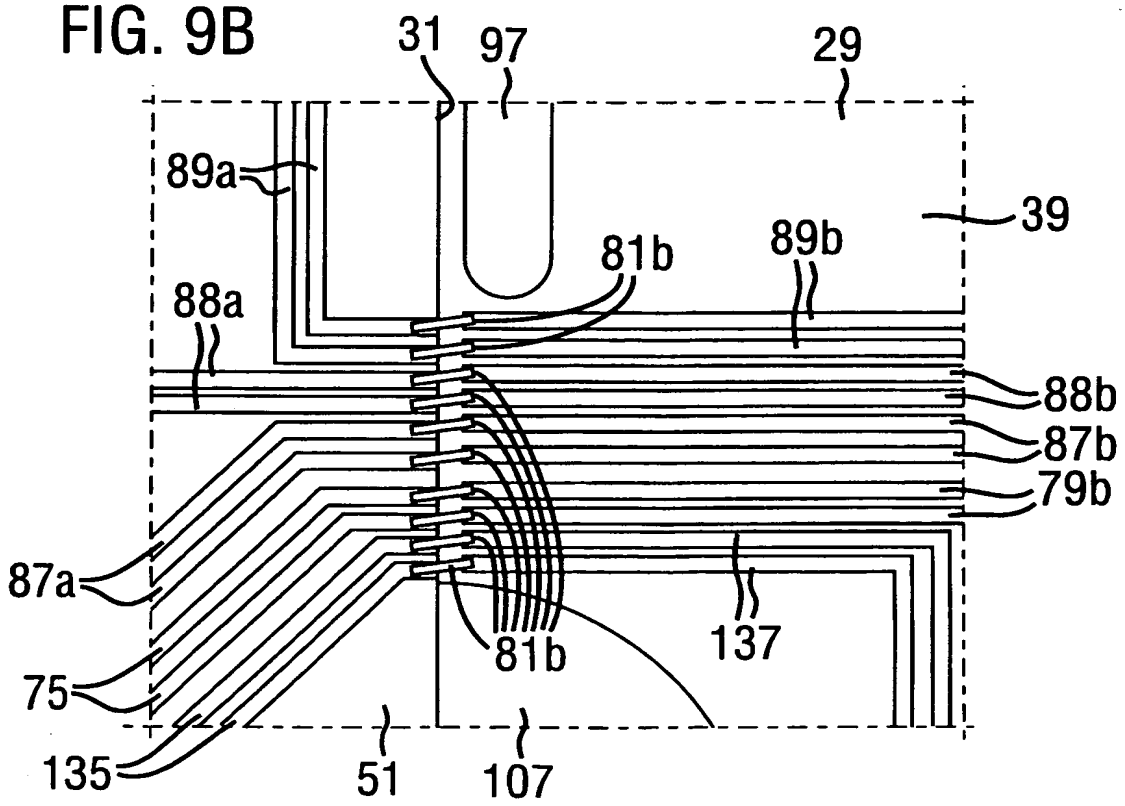

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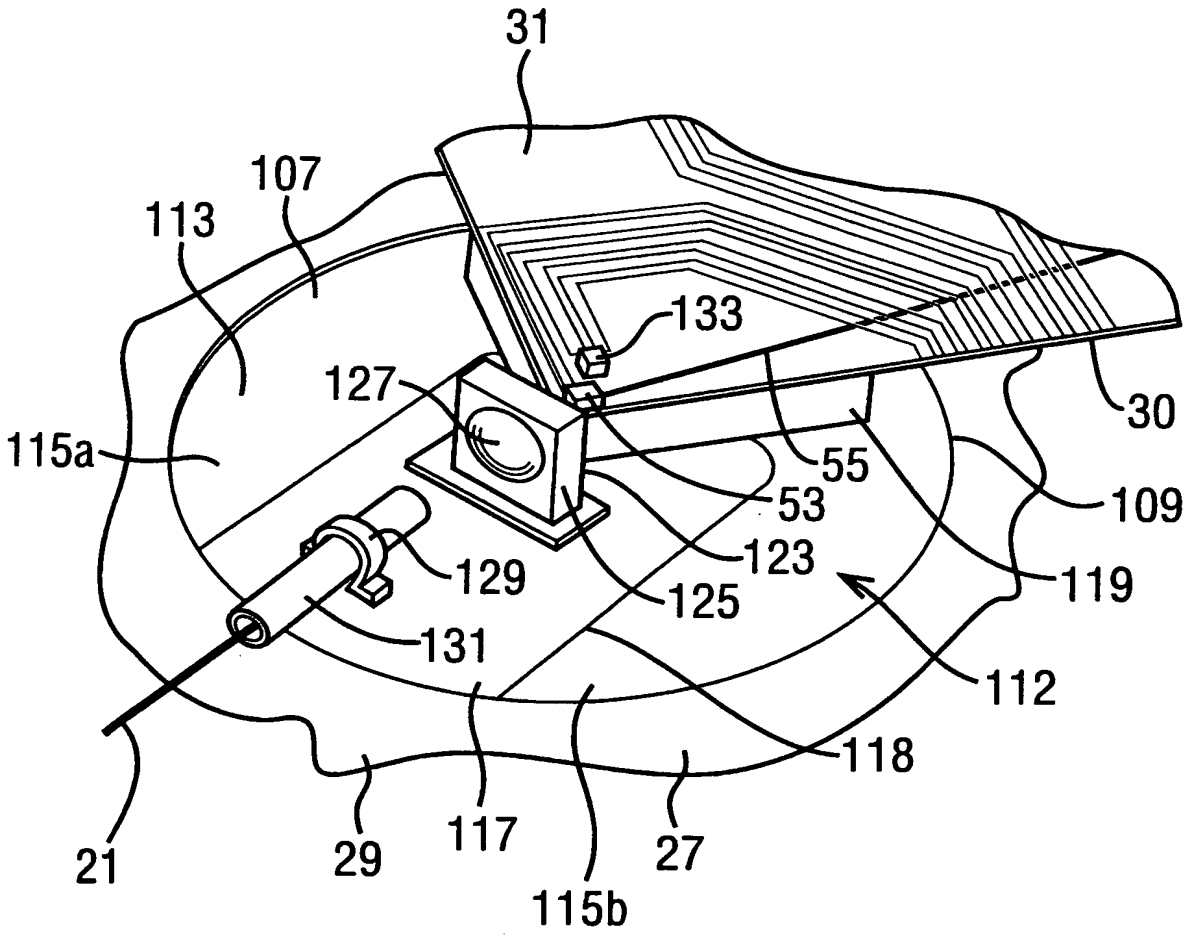
FIG. 10



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AN OPTICAL CHIP UNIT

Field of the Invention

The present invention relates to an optical chip unit having an optical chip which presents an optical circuit through which an optical signal is transmitted and a carrier member on which the optical chip is secured, and is particularly, although not exclusively, concerned with such a unit in which the optical chip has an optical circuit for processing an optical signal inputted thereto from an optical fibre, for instance demultiplexing a multiplexed input signal.

Background of the Invention

Many of the elements which make up an optical circuit need a stable temperature condition in order to function optimally, whether the optical circuit element be a passive optical element, such as an arrayed waveguide grating for demultiplexing/multiplexing optical signals, or an active optical circuit element, for instance an opto-electronic optical circuit element, such as laser diodes, or an electronic optical circuit element such as an optical amplifier or optical attenuator. To this end, the optical chip is packaged with a temperature control system for controlling the temperature of the device. Often, the temperature needs to be controlled to within close limits of an ideal operating temperature while accommodating wide fluctuations of the ambient temperature in the external environment about the package, for instance anywhere in the range of –5°C - 65°C.

An optical chip is ordinarily supported on an electrically insulating carrier member. The carrier member bulk provides a thermal conduction pathway to the optical chip, thereby making it difficult to maintain the optical circuit elements on the chip within limits of the ideal operating temperature. The aim of the present invention is to alleviate this problem.

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Summary of the Invention

According to one aspect of the invention there is provided an optical chip unit comprising an optical chip having a lower side, and a carrier member having an upper side, wherein the lower side of the optical chip is mounted on, and overlies, a first section of the upper side of the carrier member, wherein the upper side further has a second section juxtaposed to the first section, and wherein at least one cut-out is provided in the second section so as to be located adjacent the first section.

The at least one cut-out in the carrier member adjacent the optical chip acts as a barrier to heat conduction to the optical chip through the body of the carrier member, i.e. it thermally isolates the optical chip. This makes it easier to control the chip temperature, and the temperature of the optical circuit elements thereon, thereby making the chip operation more efficient.

The optical chip may have an upper side on which is provided one or more optical circuit elements, e.g. opto-electronic components such as photodiodes and laser diodes, and/or optical components such as optical waveguides and demultiplexers/multiplexers, and/or electronic components such as optical attenuators and optical amplifiers.

Preferably, the at least one-cut out is spaced from the optical chip by no less than 0.5mm or no more than 10mm. Preferably there is no spacing between the optical chip and the slot, the edge of the slot being aligned with the chip such that they are adjacent in plan view. Another design is also envisaged where the slot is spaced from the optical chip by approximately the width of the slot. Preferably the slot width is 0.5 to 5mm. The cut out may be placed at least partially underneath the edge of the chip, or even mostly underneath the chip.

Preferably, the first section is an inner section of the upper side and the second section is an outer section enclosing the inner section.

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Preferably, the upper side of the carrier member has a perimeter and the at least one cut-out is located inwardly of the perimeter.

Preferably, the lower side of the optical chip has a perimeter and the at least one cut-out generally defines at least part of an outline of the perimeter of the lower side of the optical chip. The at least one cut-out may define a polygonal outline, for instance a rectilinear, rectangular or square outline. However, radiused corners are preferred on the cut-out shape to minimise stress concentration.

The unit may have a plurality of discrete cut-outs located in the second section so as to be arranged about the first section adjacent thereto. For instance, the perimeter of the lower side of the optical chip may be composed of at least three edges, and at least two of the edges are bounded by at least one of the cut-outs. Preferably, each edge is bounded by a cut-out.

The at least one cut-out may be an elongate slot. A thin rectangle with rounded ends is the ideal shape for the cut-outs.

In an embodiment of the invention, the optical chip has an upper side and a lower side, intersecting sidewalls connecting the upper and lower sides and first and second opposed ends, wherein an optical circuit element is located on the upper side adjacent the first end and the at least one cut-out is located adjacent the sidewalls bounding the first end.

With the present invention, temperature sensitive optical circuit elements are thermally isolated from heat conduction in the carrier member, whereby the temperature of a circuit element can be more easily maintained within set temperature limits.

The second section of the upper side of the carrier member may have a plurality of discrete cut-outs arranged so that at least one of the cut-outs is provided adjacent each sidewall bounding the first end.

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The optical circuit element may be an optical demultiplexer, for instance an arrayed waveguide grating. The demultiplexer may be a multiplexer when its sense of operation is reversed.

In an embodiment of the invention, the optical chip has an upper side, a plurality of intersecting sidewalls which connect the perimeter of the upper side to the perimeter of the lower side, and at least one first electrical track on the upper side of the chip extending inwardly from the perimeter of the upper side at a first one of the sidewalls, wherein the carrier member has at least one second electrical track on its upper side which extends outwardly from a first position in the second section proximate the first sidewall, wherein the at least one cut-out extends adjacent to, and along, the first sidewall and terminates at a second position in the second section proximate the first position and wherein the first and second electrical tracks are connected to one another by an electrical connecting element. The first electrical tracks may be connected to an optical circuit element on the upper side of the chip.

The upper side of the optical chip may also have a third electrical track thereon extending inwardly from the perimeter of the upper side at a second one of the sidewalls, wherein the carrier member has at least one fourth electrical track on its upper side which extends outwardly from a third position in the second section, proximate the second sidewall, wherein at least one cut-out is provided in the second section to extend adjacent to, and along, the second sidewall and terminate at a fourth position in the second section proximate the third position and wherein the third and fourth electrical tracks are connected to one another by an electrical connecting element. Again, the third electrical tracks may be connected to an optical circuit element on the upper side of the chip.

The first position may be located between the ends of a pair of cut-outs extending adjacent to the first sidewall.

The carrier member may support at least one lead wire at its perimeter with the at least one second electrical track being connected to the at least one lead

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wire. The upper side of the carrier member may further support at least one further lead wire at its perimeter to which the at least one fourth electrical track is connected.

Preferably, the at least one cut-out extends through the carrier member from its upper side to its lower side.

The carrier member preferably has a plate-like construction. The carrier member is also preferably of a rigid construction. Typically, the carrier member is an electrical insulator. Ideally, the carrier member is formed from a ceramic material, for instance of alumina (Al_2O_3). The carrier member is further preferably gas impermeable.

In an embodiment of the invention, the first and second sections of the upper side of the carrier member collectively define a central area of the upper side which is surrounded by an outer peripheral area of the upper side, and the outer peripheral area supports a cover which encloses the central area. Preferably, the cover is gas impermeable. The cover may comprise an endless wall member mounted on the outer peripheral area and a lid member secured across the endless wall member. The cover may include at least one opening for receiving an optical fibre therethrough for coupling to the optical chip. The at least one opening may be in the wall member. Preferably, the cover is spaced inwardly of the perimeter of the upper side of the carrier member.

The cover may be a first part of a cover assembly further comprising a second part mounted to a lower side of the carrier member to enclose a central area thereof. The second part of the cover assembly is preferably gas impermeable.

The carrier member may have connector means for connecting the unit to an inner cavity of an optical package which are located outside the cover assembly.

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In an embodiment of the invention, the optical chip has an upper side on which is provided an optical circuit element which overlies a first sub-section of the first section of the upper side of the carrier member, and wherein at least one further cut-out is provided in a second sub-section of the first section which is juxtaposed to the first sub-section such that the at least one further cut-out is adjacent the first sub-section.

The optical circuit element may be a first optical circuit element with the upper side of the carrier member having a second optical circuit element spaced from the first optical circuit element to overlie a third sub-section of the first section of the upper side of the carrier member, and the at least one further cut-out is located in-between the first and second optical circuit elements.

Preferably electrical lead wires between components of the optical chip extend only over areas of the chip that are not overlying a cut-out. This minimises vibration and shock induced failures and should prevent processing failures.

According to another aspect of the present invention there is provided an optical chip unit comprising an optical chip having an upper side and a lower side, and a carrier member having an upper side, wherein the lower side of the optical chip is mounted on the upper side of the carrier member, wherein the upper side of the chip has an optical circuit element thereon overlying a first section of the upper side of the carrier member, wherein the upper side of the carrier member has a second section juxtaposed to the first section and wherein at least one cut-out is provided in the second section so as to be located adjacent the first section. The optical circuit element may be an active optical circuit element. By "active" is meant an optical circuit element whose operation is effected through a power source, typically electrical, e.g. opto-electronic and electronic components. The optical circuit element therefore tends to produce heat during use which can heat the carrier member. As examples of active circuit elements, there may be mentioned a light source such as a laser diode, an optical attenuator and an optical amplifier. The optical circuit element may be a first optical circuit element with the upper side of the optical chip having a second optical circuit element

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which overlies a third section of the upper side of the carrier member, and the at least one cut-out is located in-between the first and second optical circuit elements. The at least one cut-out thermally isolates the second optical circuit element, which may be a passive optical circuit element (i.e. unpowered), from heat conduction from the first optical circuit element through the carrier member.

The second optical circuit element may be an optical demultiplexer, an arrayed waveguide grating for example.

According to the invention there is yet further provided an optical package comprising an outer casing defining a cavity in which is housed the optical chip unit of the invention. The optical chip may have an optical circuit thereon with electrically activated circuit elements with the cavity housing an electrical control circuit for controlling the electrically activated circuit elements, said control circuit being electrically connected to said circuit elements.

An exemplary embodiment of the invention will now be described with reference to the accompanying schematic FIGURES of drawings.

Brief Description of the Drawings

FIGURE 1 is an exploded perspective view of an optical signal processing module for use in an optical communication system having an outer casing comprising a container part, in which is mounted an optical chip unit in accordance with the invention, and a lid part securable to the container part.

FIGURE 2 is a perspective view of the optical signal processing module in its assembled state.

FIGURE 3 is an exploded perspective view of the optical chip unit which has a carrier member, an optical chip secured to the carrier member and a cover assembly forming a hermetic environment about the chip.

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FIGURE 4A is a perspective view of the optical chip unit in a partially assembled state.

FIGURE 4B is a perspective view of the optical chip unit in its fully assembled state.

FIGURE 5 is a cross-sectional side view of the optical chip unit along line V-V.

FIGURE 6 is a plan view of the optical chip showing an optical signal processing circuit thereon.

FIGURE 6A is an enlarged fragmentary view of a part of the optical circuit.

FIGURE 7 is a perspective view of the carrier member of the optical chip unit.

FIGURE 8 is a plan view of the optical chip on the carrier member showing the electrical connections between electrical tracks on the optical chip and leadframes depending from the carrier member.

FIGURES 9A and 9B are enlarged fragmentary views of FIGURE 8 showing the electrical connection of the electrical tracks on the optical chip and the carrier member on the left-hand side and right-hand side, respectively.

FIGURE 10 is an enlarged fragmentary view of a corner of the optical chip showing the optical coupling of an optical fibre to an optical circuit element at the corner of the chip.

Detailed Description of the Exemplary Embodiment of the Invention

In this specification the use of terms such as "upper" and "lower" are only used for identifying the relative orientation and/or position of the features to one

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another, and not in a limiting sense. Thus, these terms are reversible or interchangeable with other similar terms, such as "front" and "rear" etc..

In the FIGURES of drawings there is shown an optical signal processing module 1 for use in processing an optical signal being transmitted in an optical communication system. Typically, the optical signal is generated by one or more lasers in remote modules of the communication system and transmitted to other modules in the communication system, including the processing module 1, by optical fibres.

In this non-limiting embodiment of the present invention, the processing module 1 takes the form of a demultiplexer (or multiplexer if reversed) for demultiplexing a multiplexed optical signal transmitted to the module 1.

Referring to FIGURES 1 and 2, the processing module 1 comprises an outer casing 2 formed by a container part 3 and a lid part 5 which, in the assembled state of the module 1, is releasably secured to the container part 3. They may be screwed together, for example. The outer casing 2 may be of metal, for instance aluminium. The container part 3 has an inner surface to which is mounted a printed circuit board (PCB) 7. In use of the module 1, the PCB 7 is connected to an electricity supply through electrical connector means 9 in the container part 3.

As shown in FIGURE 1, the PCB 7 has a cut-out 11 to reveal four props 13 upstanding from the inner surface of the container part 3. When the processing module 1 is assembled, a demultiplexing optical chip unit 15 is fixedly secured to the props 13. In use, the optical chip unit 15 is electrically connected to the PCB 7 through two leadframes 17a, 17b.

The outer casing 2 has an inlet passageway 19 for enabling a single input optical fibre 21 to be optically coupled with the optical chip unit 15 to input a multiplexed optical signal thereto, and an outlet passageway 23 for enabling a multiplicity of output optical fibres 25 arranged in a ribbon to be optically coupled to

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the optical chip unit 15 to output the demultiplexed signals therefrom. In the assembled state of the processing module 1, the optical fibres 21, 25 are positioned to face the inlet and outlet passageways 19, 23. For example, they may be fixed in place using a boot that clamps into place.

In this embodiment of the present invention, there are eight output optical fibres 25 in the ribbon. However, the skilled reader will appreciate that a lesser or greater number of output optical fibres can be used in the practice of the invention depending on the number of channels or wavelength bands to be separated from the multiplexed signal by the optical chip unit 15. The output optical fibres 25 may be single optical fibres, rather than formed into an optical fibre ribbon.

From FIGURES 1, 4A and 8 it will be seen that the output optical fibres 25 are side-mounted to the optical chip 31 through a fibre mounting block 26, as is known in the art.

Reference is now had to FIGURES 3 and 4A which show the input and output optical fibres 21, 25 connected to the optical chip unit 15. The optical chip unit 15 comprises a rigid carrier member 27 which is plate-like or sheet-like in form. The carrier member 27 is a gas impermeable, electrical insulator, preferably made from a ceramic material, most preferably a low temperature co-fired ceramic, and even more preferably alumina (Al_2O_3). When the carrier member 27 is formed from a ceramic, it is preferably formed by laser cutting from a ceramic stock sheet.

Secured to an upper side 29 of the carrier member 27 is a lower side 30 of a demultiplexer optical chip 31. In this embodiment the optical chip 31 is a hybridised integrated optical chip based on a silicon substrate, more details of which will be given shortly hereinafter. Other types of demultiplexer chip could, of course, be used.

Sealably secured on the upper side 29 of the carrier member 27 is an endless, gas impermeable wall structure 33, for example made from Kovar (RTM).

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However, any metal or alloy could be used. The wall structure 33 is sealably secured to the upper side 29 of the carrier member 27, for example by brazing or with a glass sealant, and, as shown in FIGURE 4A, divides the upper side 29 into a central section 39 which includes the optical chip 31 and a surrounding outer peripheral section 40.

As shown in FIGURES 3 and 4B, the wall structure 33 forms part of a gas impermeable upper cover 35 which further comprises a gas impermeable lid 37 which, in the assembled state, is sealably secured, for example soldered, glued or welded, or even screwed down, over the wall structure 33 to encapsulate the central section 39 of the upper side 29 of the carrier member 27. The lid may also be made of Kovar (RTM), or some other metal or alloy.

As further shown in FIGURES 3 and 4A, the wall structure 33 includes an inlet passageway 41 and an outlet passageway 43 through which the input and output optical fibres 21, 25 respectively pass for optical coupling with the optical chip 31. When the optical chip unit 15 is assembled the optical fibres 21, 25 are hermetically sealed in the passageways 41, 43, for example with a glass seal or soldering.

As will be understood from FIGURES 3 and 5, in addition to the upper cover 35 the optical chip unit 15 also has a gas impermeable lower cover 45 which may be Kovar (RTM) or ceramic, or any other sturdy metal or inorganic substance. When the optical chip unit 15 is assembled, the lower cover 45 is sealably secured to a lower side 47 of the carrier member 27, e.g. through brazing or a glass seal, to divide the lower side 47 into a central section 49 encapsulated by the lower cover 45, and an outer peripheral section 52 (see FIGURES 4A, 4B and 5). The central and outer peripheral sections 49, 52 of the lower side 47 of the carrier member 27 are in registration (co-extensive) with the central and outer peripheral sections 39, 40 of the upper side 29 of the carrier member 27.

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The upper and lower covers 35, 45 collectively form a cover assembly which provides a hermetically sealed chamber on the carrier member 27 within which is housed the optical chip 31.

As will be understood from FIGURE 6, an optical circuit 48 is provided by the optical chip 31 on an upper side 51 thereof. The principle features of the optical circuit 48 are:-

- A semiconductor optical amplifier (SOA) 53 mounted in a recess (not shown) at a corner of the chip upper side 51 at a first end 50 of the chip 31. In this particular embodiment, the SOA 53 is a linear optical amplifier (LOA), for example, one sold by Genoa Corporation. The LOA 53 is block-like in form having electrically conducting legs (not shown) depending from a lower side thereof which stand in the recess to space the underside above the chip upper side 51. The underside of the LOA 53 further has a rib-like optical waveguide (not shown) formed thereon.

- A rib-like input optical waveguide 55 formed by a silicon-on-insulator (SOI) technique on the silicon substrate of the chip 31, as is known in the art (see e.g. WO95/08787). The input waveguide 55 is optically coupled at its inlet end 57 to the LOA waveguide, and its outlet end 58 terminates at a position towards a second end 59 of the optical chip 31 opposite the first end 50.

- An optical demultiplexer 61 defined by an arrayed waveguide grating (AWG), such as disclosed in US-A-5002350. The AWG 61 is also formed on the silicon substrate of the optical chip 31 by a SOI technique. The AWG 61 has an inlet end 63 adjacent to, but separated by a free space region 64 from, the outlet end 58 of the input waveguide 55. It also has an outlet end 65. The free space region is also known as a star coupler.

- An array of rib-like output optical waveguides 67 formed by a SOI technique, each extending from an inlet end 68 disposed adjacent to, but spaced by a free space region 69 from, the outlet end 65 of the AWG 61 to an outlet end 71 at

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the perimeter of the chip upper side 51 at the first chip end 50. The number of output waveguides 67 matches the number of output optical fibres 25. So, in this instance, there are eight output waveguides 67.

- A variable optical attenuator (VOA) 73 in which PIN diodes are formed laterally about each output waveguide 67 so that, when the PIN diodes are biased, the charge carrier movement in the diodes alters the refractive indices of the output optical waveguides 67 thereby attenuating the respective optical signals. Reference may be made to Bookham Patent Application Nos. PCT/GB02/01899 and GB0110278.9 and publication number GB-A-2367142, for example, the contents of which are hereby incorporated by reference.

- Electrically conducting tracks 75, 77 extending from the LOA 53 and the VOA 73 to the perimeter of the chip upper side 51. The tracks 75, 77 may be formed by metallization, as known in the art.

The general operation of the optical circuit 48 is as follows. First, the input optical fibre 21 inputs a multiplexed optical signal into the LOA 53 where it is amplified. The amplified multiplexed signal is then transmitted along the input waveguide 55 and transferred from the outlet end 58 thereof to the inlet end 63 of the AWG 61. The AWG 61 divides the multiplexed optical signal into eight optical signals (demultiplexed signals) of different wavelength bands. The demultiplexed signals are transmitted from the outlet end 65 of the AWG 61 on transmission paths which are angularly separated from one another. The inlet ends 68 of the output waveguides 67 are respectively aligned with a different transmission path, whereby the demultiplexed signals are collected in a different output waveguide 67. The demultiplexed signals in the output waveguides 67 are then processed by the VOA 73 so that the power levels of the demultiplexed signals at the respective outlet ends 71 of the output waveguides 67 are the same, or substantially the same.

As will be understood by a skilled reader, the operation of the optical circuit 48 can be reversed so that the optical chip 31 functions as a multiplexer. In short,

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eight optical signals of different wavelength bands are inputted to the VOA 73 for variable attenuation thereof so that the optical signals are transferred to the AWG 61 with the same power. The AWG 61 then combines the optical signals into a single multiplexed signal which is then amplified by the LOA 53 before onward transmission in the optical fibre communication system.

As shown in FIGURE 8, individual leads of the leadframes 17a, 17b are connected to electrical tracks 79a, 79b formed on the upper side 29 of the carrier member 27, e.g. by metallization. The electrical tracks 79a, 79b extend from the associated leadframe 17a, 17b to positions adjacent first and second opposed sides of the optical chip 31. The electrical tracks 75, 77 on the chip upper side 51 for the LOA 53 and the VOA 73 respectively extend to the perimeter of the chip upper side 51 at the first and second sides. As shown in FIGURES 9A and 9B, the electrical tracks 75, 77 for the LOA 53 and VOA 73 are electrically connected to the adjacent electrical tracks 79a, 79b on the upper side 29 of the carrier member 27 by wire bonds 81a, 81b, respectively. In this way, the LOA 53 and the VOA 73 are electrically connected to leads in the associated leadframe 17a, 17b.

When the optical chip unit 15 is mounted in the container part 3 of the outer casing 2, the leadframes 17a, 17b are connected to the electrical circuit on the PCB 7, e.g. by soldering. The electrical circuit comprises control means for controlling the operation of the LOA 53 and the VOA 73 via the leadframes 17a, 17b and associated electrical tracks 75, 77, 79a, 79b.

For the VOA 73 and AWG 61 to operate efficiently, it is necessary for these optical circuit elements to be maintained within close limits of their ideal operating temperature, irrespective of ambient temperature fluctuations outside the optical chip unit 15. To this end, and as shown in FIGURES 3 and 5, the central section 49 of the lower side 47 of the carrier member 27 carries a first thermoelectric cooler (TEC) 91 in close proximity to, and in close thermal contact with the VOA 73, and a second TEC 93 in close proximity to, and in close thermal contact with the AWG 61. The TECs 91, 93 are electrically connected to the control means of the PCB circuit so that the control means can control their operation. Preferably

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the TECs 91, 93 are positioned inside the chamber to provide advantages in the robustness of the unit. The TECs 91, 93 could, however, also be positioned above the chip 31, below the lid 35, or outside the chamber, e.g. below thermally conducting elements 101, 103.

Mounted to each TEC 91, 93 is a thermally conducting element 101, 103, for instance made from a metal such as CuW, a copper tungsten alloy. The thermally conducting elements 101, 103 are sealingly inserted into apertures 94a, 94b in the lower cover 45. When the optical chip unit 15 is mounted on the props 13 on the inner surface of the container part 3 of the outer casing 2, the thermally conducting elements 101, 103 are thermally connected to a heat sink 95 (see FIGURES 1 and 2) provided on the external surface of the container part 3. The thermally conducting elements 101, 103 may be above or below the TECs 91, 93. They are shown below the TECs 91,93, the TECs thermally coupling the thermally conducting elements 101, 103 to carrier member 27 by the VOA 73 and the AWG 61. However, the positions of the TECs 91, 93 and the thermally conducting elements 101, 103 could be swapped around, with the TECs 91, 93 below the sealing thermally conducting elements 101, 103.

As shown in FIGURE 2, the heat sink 95 in this embodiment takes the form of a series of spaced-apart, recessed fins or plate-like elements integrally formed in the outer casing 2. Other forms of heat sink could, of course, be used.

It will be appreciated that the TECs 91, 93 operate to transfer heat from the VOA 73 and AWG 61 to the heat sink 95 through the thermally conducting elements 101, 103, thereby acting to maintain the temperature of the VOA 53 and AWG 61 within close limits of their ideal operating temperature for efficient operation thereof. In this regard, the optical circuit 48 further comprises temperature sensors 83, 84, 85 for monitoring the temperature of the VOA 73 and the AWG 61. As will be understood from FIGURES 6, 8 and 9B, the temperature sensors 83, 84, 85 are electrically connected to the control means on the PCB 7 through wire-bonded pairs of electrical tracks 87a, 87b; 88a, 88b; 89a, 89b on the optical chip 31 and carrier member 27 which are electrically connected to other

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leads in the leadframe 17b. In this way, the control means is able to vary the electrical control signals sent to the TECs 91, 93 in dependence of the temperature measurement signals from the temperature sensors 83, 84, 85.

It is especially important to maintain the AWG 61 within close limits of its ideal operating temperature, otherwise wavelength drift is caused in the demultiplexing operation. This can result in the output waveguides 67 carrying optical signals of incorrect wavelength.

Mindful of the need to keep the operating temperature of the AWG 61 within close limits of its ideal, it will be seen from FIGURES 4A, 7 and 8 that the carrier member 27 has a number of discretely arranged, unfilled or void slots 97 which (i) extend from the central section 39 of the upper side 29 of the carrier member 27 to the central section 49 of the lower side 47, and (ii) are disposed adjacent to, and extend along, the perimeter of the optical chip 31. The slots 97 act to thermally isolate the optical chip 31 from the outer peripheral sections 40, 52 of the carrier member 27 which are used to mount the chip unit 15 to the container part 3 of the outer casing 2 of the module 1, and hence exposed to the interior environment of the outer casing 2, including its ambient temperature which may differ from that desired inside the sealed environment provided about the optical chip 31 by the cover assembly 35, 45. With this in mind, the thermal isolation slots 97 reduce the number of thermal conduction paths to the optical chip 31 through the body of the carrier member 27 from its perimeter.

Due the sensitivity of the AWG 61 to temperature fluctuations, the thermal isolation slots 97 are concentrated around the three sides of the optical chip 31 which bound the end 59 of the optical chip 31 at which the AWG 61 is located.

The slots 97 are preferably made as large as possible whilst leaving enough residual material or lands to support the optical chip 31, the leadframes 17a, 17b and the electrical tracks connecting the optical circuit 48 on the chip 31 to the leadframes 17a, 17b.

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In addition to the slots 97 arranged externally adjacent the perimeter of the optical chip 31, a number of slots 99 may also be made in the carrier member 27 underneath the optical chip 31, for instance adjacent the perimeter of the VOA 73 between the VOA 73 and the AWG 61, as shown in dotted line in FIGURE 8 and labelled 99. Of course, similar slots could be arranged adjacent the LOA 53 between it and the AWG 61.

The slots 97, 99 in the carrier member 27 are preferably formed by laser cutting.

In addition to the TECs 91, 93, the sealed interior environment of the optical chip unit 15 may also house heating elements (not shown) to regulate the temperature therein under control of the control means of the PCB circuit.

As will be seen in FIGURES 3, 4A, 7, 8 and 10, the carrier member 27 includes a disc-shaped thermal conductor insert 107 made from a material with a higher coefficient of thermal conductivity than that of the material of the carrier member 27. In this instance a metal is used, although other materials can, of course, be used instead. The metallic insert 107 is bonded into a complementary slot 109 formed in the carrier member 27, e.g. by soldering. The slot 109 can be cut by laser cutting. Soldering minimises external stress and pressure on the chip, transferring it instead to the carrier member 27. This is advantageous because stress applied to the chip would cause problems with optical performance and would be detrimental to the functioning of the device.

As shown in FIGURE 5, the insert 107 protrudes from the lower side 47 of the carrier member 27 to be sealingly received in an aperture 111 in the lower cover 45 of the optical chip unit 15. The insert 107 carries a third thermoelectric cooling device (TEC) 110 on its underside which, in the assembled state of the module 1, is thermally connected to the heat sink 95 on the outer casing 2.

Referring particularly to FIGURE 10, in this embodiment the insert 107 has a metallic first part 112 comprising a generally U-shaped metallic outer section 113

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having a pair of limbs 115a, 115b, and a metallic inner section 117 disposed between the limbs 115a, 115b. The outer and inner sections 113, 117 of the first part 112 of the insert 107 are of dissimilar metals, with the outer section 113 preferably being formed from a copper tungsten alloy (CuW) having a high thermal conductivity, and the inner section 117 preferably formed from Kovar (RTM), an alloy of nickel (Ni), cobalt (Co) and iron (Fe) having a low thermal conductivity. The metallic outer and inner sections 113, 117 are joined together by brazing at 118. The carrier member 27 is a ceramic having a low thermal conductivity, but not necessarily lower than the Kovar (RTM).

The slot 109 for the insert 107 is located in the carrier member 27 so that the corner of the optical chip 31 carrying the LOA 53 overhangs the slot 109. It will be seen that the first part 112 of the insert 107 is recessed below the upper side 29 of the carrier member 27. It will further be seen that the insert 107 has a second part 119 seated on the first part 112 so as to support the overhanging corner of the optical chip 31. In this connection, the second part 119 is of complementary shape to the corner, i.e. triangular. The second part 119 is preferably also of a metal, most preferably a CuW alloy. The first and second parts 112, 119 may also be conjoined by brazing.

The lower side 30 of the optical chip 31 is adhered to the upper side 29 of the carrier member 27 at adhesive zones indicated by reference numerals 121a, 121b, 121c in FIGURE 7. As will be understood from FIGURE 5, the lower side 30 of the chip 31 is also spaced from the carrier member 27 by a few micrometres by a number of pillars 122 formed from a dielectric material, such as a glass. Correspondingly, the second part 119 of the insert 107 stands proud of the upper side 29 of the carrier member 27, and the corner of the optical chip 31 is adhered to the second part 119 through an adhesive layer 124 (FIGURE 7) having a relatively good thermal conductivity. The corner of the optical chip 31 is spaced from the upper side 29 of the carrier member 27 by the second part 119 (with its adhesive layer 124) by approximately the same distance as achieved by the pillars 122.

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Preferably the chip 31 rests on its corner (see Figure 10) on the second part 119 of the insert 107. This second part 119 acts as a first leg. This leg is thermally conductive and preferably made of a copper tungsten alloy (CuW). The rest of the chip is then supported by just two other legs 122 (e.g. see Figure 5). The legs are preferably made of a ceramic or glass material. Because just then three legs support the chip 31, the chip will sit firmly on all three legs. Therefore a very thin adhesive layer 124 can be used. Therefore there is a minimal contact distance between the first leg and the chip, thereby reducing its thermal resistance; adhesive is less thermally conductive than CuW. Also, because the adhesive layer 124 is thin, it will set as a very stiff layer, i.e. it will have a high Young's modulus. This provides a stable platform for aligning the optical fibre 21 with the LOA 53.

As shown in FIGURE 10, the inner section 117 of the first part 112 of the insert 107 is used to support a lens assembly 123 comprising a metal lens mount frame 125 and a lens 127 in the frame 125. The inner section 117 further supports a metal fibre mount assembly 129 having a ferrule 131 in which the free end of the input optical fibre 21 is secured.

The outer section 113 of the first part 112 of the insert 107, and the second part 119 of the insert 107, are made from CuW due to the good thermal conductivity of this metal alloy. While Kovar (RTM) has a lower coefficient of thermal conductivity than CuW, it is easier to weld articles to it. Thus, Kovar (RTM) is selected for the inner section 117 of the first part 112 of the insert 107 to allow the lens frame 125 and fibre mount assembly 129 to be welded to it, e.g. by laser welding. In use of the processing module 1, the lens 127 directs the multiplexed signal emitted from the input optical fibre 21 to the waveguide of the LOA 53 so that the multiplexed signal is amplified prior to its transfer to the input waveguide 55.

As will be appreciated, the operation of the LOA 53 results in heat production at the corner of the optical chip 31 overhanging the insert 107. However, the insert 107 conducts the heat to the heat sink 95 via the third TEC

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110, thereby controlling the temperature at the LOA 53 so that its performance is optimised.

To this end, as shown in FIGURES 6, 8 and 9B, a temperature sensor 133 is positioned on the chip corner adjacent the LOA 53 and electrically connected to the PCB control circuit through a pair of wire-bonded electrical tracks 135, 137 and associated leads in the leadframe 17b. Thus, the operation of the third TEC 110, and hence the heat extraction rate from the chip area of the LOA 53 by the thermal conductor insert 107, is controlled by the PCB control circuit in dependence of the temperature measurement signals received from the LOA temperature sensor 133.

It will be gathered from the foregoing description that the temperature regulation of the optical circuit elements 53, 61, 73 on the optical chip 31 is made easier through the provision of the thermal isolation slots 97, 99, especially the temperature regulation of the AWG 61. Moreover, the temperature regulation of the LOA 53 is made easier by overhanging the chip corner on the thermal conductor insert 107. In fact, the slots 97 and the thermal conductor insert 107 help the temperature in the optical chip unit 15 to be maintained at, or within close limits of, room temperature (25°C) for any ambient temperature in the external environment to the processing module 1 in the range of –5°C to 65°C.

It will be understood that the present invention is not limited to the embodiment described with reference to the accompanying FIGURES of drawings, but can be modified and varied in many ways within the scope of the appended claims.

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CLAIMS

1. An optical chip unit comprising an optical chip having a lower side, and a carrier member having an upper side, wherein the lower side of the optical chip is mounted on, and overlies, a first section of the upper side of the carrier member, wherein the upper side further has a second section juxtaposed to the first section, and wherein at least one cut-out is provided in the second section so as to be located adjacent the first section.

2. A unit according to claim 1, wherein the first section is an inner section of the upper side and wherein the second section is an outer section enclosing the inner section.

3. A unit according to claim 1 or 2, wherein the upper side of the carrier member has a perimeter and the at least one cut-out is located inwardly of the perimeter.

4. A unit according to claim 1, 2 or 3, wherein the lower side of the optical chip has a perimeter and wherein the at least one cut-out defines an outline of the perimeter of the lower side of the optical chip.

5. A unit according to any one of the preceding claims having a plurality of discrete cut-outs located in the second section so as to be arranged about the first section adjacent thereto.

6. A unit according to claim 5 when appended to claim 4, wherein the perimeter of the lower side of the optical chip is composed of at least three edges, and wherein at least two of the edges are bounded by at least one of the cut-outs.

7. A unit according to any one of claims 1 to 4, wherein the optical chip has an upper side, intersecting sidewalls connecting the upper and lower sides and first and second opposed ends, wherein an optical circuit element is located on the

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upper side adjacent the first end, and wherein the at least one cut-out is located adjacent the sidewalls bounding the first end.

8. A unit according to claim 7, wherein the second section has a plurality of discrete cut-outs arranged so that at least one of the cut-outs is provided adjacent each sidewall bounding the first end.

9. A unit according to claim 7 or 8, wherein the optical circuit element is an optical demultiplexer.

10. A unit according to claim 9, wherein the optical demultiplexer is an arrayed waveguide grating.

11. A unit according to any one of claims 1 to 4, wherein the optical chip has an upper side, a plurality of intersecting sidewalls which connect the perimeter of the upper side to the perimeter of the lower side, and at least one first electrical track on the upper side of the chip extending inwardly from the perimeter of the upper side at a first one of the sidewalls, wherein the carrier member has at least one second electrical track on its upper side which extends outwardly from a first position in the second section proximate the first sidewall, wherein the at least one cut-out extends adjacent to, and along, the first sidewall and terminates at a second position in the second section proximate the first position and wherein the first and second electrical tracks are connected to one another by an electrical connecting element.

12. A unit according to claim 11, wherein the first electrical tracks are connected to an optical circuit element on the upper side of the chip.

13. A unit according to claim 11 or 12, wherein the upper side of the optical chip has at least one third electrical track thereon extending inwardly from the perimeter of the upper side at a second one of the sidewalls, wherein the carrier member has at least one fourth electrical track on its upper side which extends outwardly from a third position in the second section proximate the second

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sidewall, wherein at least one cut-out is provided in the second section to extend adjacent to, and along, the second sidewall and terminate at a fourth position in the second section proximate the third position and wherein the third and fourth electrical tracks are connected to one another by an electrical connecting element.

14. A unit according to claim 13, wherein the third electrical tracks are connected to an optical circuit element on the upper side of the chip.

15. A unit according to any one of claims 11 to 14, wherein the first position is located between the ends of a pair of cut-outs extending adjacent to the first sidewall.

16. A unit according to any one of claims 11 to 15 , wherein the carrier member supports at least one lead wire at its perimeter and the at least one second electrical track is connected to the at least one lead wire.

17. A unit according to claim 16 when appended to claim 13 or 14, wherein the upper side of the carrier member supports at least one further lead wire at its perimeter and the at least one fourth electrical track is connected to the at least one further lead wire.

18. A unit according to any one of the preceding claims, wherein the at least one cut-out extends through the carrier member.

19. A unit according to any one of the preceding claims, wherein the carrier member has a plate-like construction.

20. A unit according to any one of the preceding claims, wherein the carrier member is of a rigid construction.

21. A unit according to any one of the preceding claims, wherein the carrier member is an electrical insulator.

22. A unit according to any one of the preceding claims, wherein the carrier member is formed from a ceramic material.

23. A unit according to any one of the preceding claims, wherein the carrier member is gas impermeable.

24. A unit according to any one of the preceding claims, wherein the first and second sections of the upper side of the carrier member collectively define a central area of the upper side which is surrounded by an outer peripheral area of the upper side, and wherein the outer peripheral area supports a cover which encloses the central area.

25. A unit according to claim 24, wherein the cover is gas impermeable.

26. A unit according to claim 24 or 25, wherein the cover comprises an endless wall member mounted on the outer peripheral area and a lid member secured across the endless wall member.

27. A unit according to any one of claims 24 to 26, wherein the cover includes at least one opening for receiving an optical fibre therethrough for coupling to the optical chip.

28. A unit according to any one of claims 24 to 27, wherein the cover is spaced inwardly of the perimeter of the upper side of the carrier member.

29. A unit according to any one of claims 24 to 28, wherein the cover is a first part of a cover assembly further comprising a second part mounted to a lower side of the carrier member to enclose a central area thereof.

30. A unit according to claim 29, wherein the carrier member has connector means for connecting the unit to an inner cavity of an optical package which are located outside the cover assembly.

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31. A unit according to claim 29 or 30, wherein the second part of the cover assembly is gas impermeable.

32. A unit according to any one of claims 1 to 6, wherein the optical chip has an upper side on which is provided an optical circuit element which overlies a first sub-section of the first section of the upper side of the carrier member, and wherein at least one further cut-out is provided in a second sub-section of the first section which is juxtaposed to the first sub-section such that the at least one further cut-out is adjacent the first sub-section.

33. An optical chip unit comprising an optical chip having an upper side and a lower side, and a carrier member having an upper side, wherein the lower side of the optical chip is mounted on the upper side of the carrier member, wherein the upper side of the chip has an optical circuit element thereon overlying a first section of the upper side of the carrier member, wherein the upper side of the carrier member has a second section juxtaposed to the first section and wherein at least one cut-out is provided in the second section so as to be located adjacent the first section.

34. A unit according to claim 32 or 33, wherein the optical circuit element is an active optical circuit element.

35. A unit according to claim 34, wherein the optical circuit element is selected from the group consisting of a light source, an optical attenuator and an optical amplifier.

36. A unit according to claim 32 or one of claims 34 and 35 when appended to claim 32, wherein the optical circuit element is a first optical circuit element and the upper side of the carrier member has a second optical circuit element spaced from the first optical circuit element to overlie a third sub-section of the first section of the upper side of the carrier member, and wherein the at least one further cut-out is located in-between the first and second optical circuit elements.

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37. An optical chip unit according to claim 33 or one of claims 34 or 35 when appended to claim 33, wherein the optical circuit element is a first optical circuit element, wherein the upper side of the optical chip has a second optical circuit element which overlies a third section of the upper side of the carrier member and wherein the at least one cut-out is located in-between the first and second optical circuit elements.

38. A unit according to claim 36 or 37, wherein the second optical circuit element is an optical demultiplexer.

39. A unit according to claim 38, wherein the demultiplexer is an arrayed waveguide grating.

40. A unit according to any one of the preceding claims, wherein electrical lead wires between components of the optical chip extend only over areas of the chip that are not overlying a cut-out.

41. An optical package comprising an outer casing defining a cavity in which is housed the optical chip unit of any one of the preceding claims.

42. A package according to claim 41 in which the optical chip has an optical circuit thereon with electrically activated circuit elements and wherein the cavity houses an electrical control circuit for controlling the electrically activated circuit elements, said control circuit being electrically connected to said circuit elements.

43. An optical chip unit substantially as hereinbefore described with reference to, and as illustrated in, the accompanying FIGURES of drawings.

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Application No: GB 0219887.7 **Examiner:** Emily McGeehin
Claims searched: 1 and 33 at least **Date of search:** 8 April 2003

Patents Act 1977 : Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance	
X	1 to 6, 8 to 10, 18 to 20, 22, 24, 30, 32 to 35 and 41	EP 413182 A2	GTE LABORATORIES INC Abstract Figures 3a, 3b and 5 Column 1, lines 1 to 18 Column 4, lines 4 to 7 and 43 to 47 Column 5, line 53 to column 6, line 33 Column 6, lines 10 to 14 and 19 to 23 Column 8, line 46 to column 9, line 40 Column 9, lines 17 to 40 Column 10, lines 12 to 15 Column 12, lines 44 to 48
A		US 2002/0071188 A1	AOKI AND MATSUURA Figures 1, 4, 5 and 10 Paragraphs, 0022 to 0024, 0027, 0032 and 0040

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
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Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC[V]:

H1K

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H01L, H01S, G02B

The following online and other databases have been used in the preparation of this search report :

EPODOC, WPI, JAPIO, INSPEC

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